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IN THE CLAIMS

1. (Currently amended) A semiconductor device comprising:

a device isolation layer disposed in a substrate to define an active region;

source and drain regions formed in the active region;

a gate electrode formed on the active region between the source and drain regions;

a gate insulation layer interposed between the gate electrode and the active region;

a resistor pattern formed on the device isolation layer;

resistor spacers disposed on sidewalls of the resistor pattern; and

an interlayer dielectric layer disposed over the resistor pattern; and

resistor electrodes connected to both ends of the resistor pattern, respectively, wherein the gate electrode includes a polysilicon layer and a silicide layer that are sequentially stacked on the gate insulation layer, wherein the resistor pattern includes a single-layer polysilicon layer, wherein substantially the entire resistor pattern does not have a silicide layer disposed thereon, and wherein the resistor spacer protrudes above the resistor pattern, and wherein the interlayer dielectric layer contacts a portion of the resistor spacer.

2. (Currently amended) The device of claim 1, wherein the gate insulation layer is multi-layered and includes at least one ~~silicon nitride~~ charge storage dielectric layer.

3. (Original) The device of claim 1, wherein the resistor pattern is in direct contact with the device isolation layer.

21. (New) The device of claim 1, wherein the gate insulation layer is multi-layered and includes at least one charge storage dielectric layer.

22. (New) The device of claim 21, wherein the charge storage dielectric layer comprises silicon nitride.

23. (New) The device of claim 2, wherein the charge storage dielectric layer comprises silicon nitride.

24. (New) A semiconductor device comprising:

a device isolation layer disposed in a substrate to define an active region;

source and drain regions formed in the active region;

a gate electrode formed on the active region between the source and drain regions;

a gate insulation layer interposed between the gate electrode and the active region;

a resistor pattern formed on the device isolation layer;

resistor insulating spacers disposed on sidewalls of the resistor pattern, each resistor insulating spacer having a vertical inner sidewall;

an interlayer dielectric layer disposed over the resistor pattern; and

resistor electrodes connected to both ends of the resistor pattern, respectively, wherein the gate electrode includes a polysilicon layer and a silicide layer that are sequentially stacked on the gate insulation layer, wherein the resistor pattern includes a single-layer polysilicon layer, wherein substantially the entire resistor pattern does not have a silicide layer disposed thereon, wherein the resistor spacer protrudes above the resistor pattern, and wherein the interlayer dielectric layer contacts a portion of the vertical inner sidewall of the resistor insulating spacers.